REMARKS

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this application in view of the foregoing amendment and the following remarks. The Applicants originally submitted Claims 1-35 in the application. In response to the Office Action dated May 1, 2002, the Applicants elected to prosecute the invention of a method Group I, namely Claims 1-28. In response to the present Examiner's Action, the Applicants have amended Claims 1, 4, 10, 12-14, 23 and canceled Claims 2-3, 6-7, 10 and 15-16, 18-19 and 25 without prejudice or disclaimer. The amendments to Claims 1, 14, and 23 are fully supported by the canceled claims, the specification (Page 7 Lines 29-32 and FIGURE 9, for example) and by U.S. patent application 09/637,069 now issued as U.S. Patent No. 6,355,498 to Chan *et al.* (FIGURE 9, for example). Accordingly, Claims 1, 4, 8-9, 11-14, 17, 20-23, 26-28 are currently pending in the application.

I. Objection

The Examiner has objected to the specification as containing a typographical error in the paragraph beginning on page 6, line 6. In response, the Applicants have amended the specification to correct this inadvertent error as suggested by the Examiner.

II. Rejection of Claims 1-28, under 35 U.S.C. §103

The Examiner has rejected Claims 1-6, 11-18, 22-24 and 28 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,853,601 to Krishaswamy *et al.* ("Krishaswamy") in view of U.S. Patent No. 5,998,861 to Nakaki *et al.* ("Nakaki"). The Examiner further rejected Claims 7, 10, 19 and 25 under 35 U.S.C. §103(a) as being unpatentable over Krishaswamy in view of

Nakaki and further in view of U.S. Patent No. 6,093,330 to Chong *et al.* ("Chong"). The Examiner also rejected Claims 8, 20 and 26 under 35 U.S.C. §103(a) as being unpatentable over Krishaswamy in view of Nakaki and further in view of U.S. Patent No. 6,131,256 to Dydyk *et al.* ("Dydyk 256"). The Examiner also rejected Claims 9, 21 and 27 under 35 U.S.C. §103(a) as being unpatentable over Krishaswamy in view of Nakaki and further in view of U.S. Patent No. 5,424,698 to Dydyk *et al.* ("Dydyk 698").

The Applicants respectfully maintain that the claimed invention is not obvious in view of the foregoing references, and that these references fail to establish a *prima facie* case of obviousness.

First, the combination of Krishaswamy and Nakaki fail to teach or suggest all elements of independent Claims 1, 14 and 23. For example, neither Krishaswamy nor Nakaki alone or in combination teach or suggest forming a plurality of substantially circular holes on opposing sides and through the RF component at least to the semiconductor substrate, as recited in Claim 1, 14 and 23. Nor do these references recite the diameter ranges and ranges of uniform spacing between openings, as recited in these claims. Rather, Krishaswamy (FIGURE 6) and Nakaki (FIGURE 1A) form two rectangular or L-shaped trenches, respectively, that extend substantially the length of the substrate. Moreover, one who is skilled in the art would not be motivated to form the openings in the way recited in the presently claimed inventions, because Krishaswamy teaches a very controlled process that requires an etch time of 125 minutes performed in segments to prevent the photoresist etch mask from polymerizing. (Col. 3, lines 55-60, Col. 5, lines 59-67 and Col. 6, lines 1-10). If the openings were formed as suggested by the Examiner, it could substantially increase the etch rate such that the resulting air gap is not uniform as is desired by the teachings of Krishaswamy. (Col. 6, lines 55-58). It should be noted that the claimed etching vias provide a much faster etch rate than that disclosed in Krishaswamy. Nakaki does nothing to cure the deficient and

antithetic teachings of Krishaswamy Thus, the combination fails to establish a prima facie case of obviousness.

None of Chong, Dydyk 256 nor Dydyk 698 remedy these deficient teachings. FIGURE 15 in Chong also depicts two rectangular via channels 86, 88 that extend substantially the length of the substrate. Chong teaches the use of SF_6 as etchant (Column 9, Lines 66-67). Dydyk 256 and Dydyk 698 were cited by the Examiner for the proposition of teaching Al electrodes and SiN insulators, respectively, and not for teaching any aspects of top side etching.

In addition, the Applicants respectfully maintain that the combination of Krishaswamy and Nakaki is improper because there would be no motivation for one of ordinary skill to combine Nakaki's teaching of using xenon difluoride as the etchant with Krishaswamy. *See* M.P.E.P. ¶706.02(j). As noted above, Krishaswamy is concerned with preventing polymerization of the photoresist during etching. It follows therefore that Krishaswamy would not be motivated to change etchants to a xenon difluoride because this would require undue experimentation to arrive at the conditions, if any, that would allow etching of the substrate without polymerizing Krishaswamy's photoresist. Furthermore, Nakaki is explicit about the gases that can be used. For example, Nakaki teaches using a fluoride of a rare gas or a fluoride of a haloid (Col. 3, lines 32-33 and Col. 4, lines 1-5), and it even limits the materials that can be used, depending on its resistance to xenon difluoride gas. (Col. 5, lines 1-5). Given the explicit teachings of Nakai, one who is skilled in the art would not be motivated to replace one gas with another without a suggestion or motivation to do so. There is no teaching in either reference that provides such a suggestion or motivation.

Because Krishaswamy and Nakaki alone or in combination do not teach or suggest all elements of independent Claims 1, 14 and 23 and are not properly combinable, they fail to establish

a *prima facie* case of obviousness with respect to independent Claims 1, 14 and 23and their respective dependent claims.

III. Conclusion

In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1, 4, 8-9, 11-14, 17, 20-23, 26-28.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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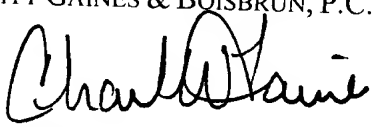

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

(1) The paragraph beginning on page 6, line 6 has been amended as follows:

A conductive layer 13 is then formed using conventional techniques on the dielectric layer 11 (FIG. 3). The conductive layer 13 may [the] be patterned to define an RF component 10, as shown in FIGS. 4 and 5. Again, conventional lithographic and etch techniques known in the art may be used to pattern the conductive layer 13. The conductive layer may be aluminum, for example, although those of skill in the art will appreciate that other suitable conductors may be used as well. The conductive layer 13 of a typical RF component may be patterned to be an inductor or a capacitor, for example, though other circuit configurations are also possible.

IN THE CLAIMS:

(1) Kindly amend Claim 1 as follows:

1. (Amended) A method for making a radiofrequency (RF) component comprising:

forming a dielectric layer on a semiconductor substrate;

forming and patterning a conductive layer on the dielectric layer to define the RF component;

forming a plurality of openings on opposing sides and [at least one opening] through the RF component at least to the semiconductor substrate, the openings having a diameter ranging from about 0.5 to about 20 microns and substantially uniform spacing between adjacent openings in a range of about 20 to about 200 microns; and

releasing the RF component from the semiconductor substrate by exposing the semiconductor substrate to [an] a dry etchant comprising XeF_2 passing through the at least one opening to the semiconductor substrate.

(2) Kindly cancel Claims 2-3 without prejudice or disclaimer.

(3) Kindly amend Claim 4 as follows:

4. (Amended) The method of Claim 1 wherein [forming] the [at least one opening comprises forming, a plurality of] openings are laterally adjacent portions of the conductive layer with no openings extending through the conductive layer.

(4) Kindly cancel Claims 6-7 and 10 without prejudice or disclaimer.

(5) Kindly amend Claim 12 as follows:

12. (Amended) The method of Claim 1 where in the openings extend [at least one opening extends] into the semiconductor substrate.

(6) Kindly amend Claim 13 as follows:

13. (Amended) The method of Claim 1 wherein the openings [at least one opening] substantially terminate [terminates] at a surface of the semiconductor substrate.

(7) Kindly amend Claim 14 as follows:

14. (Amended) A method for making a radio frequency (RF) component comprising:

forming a dielectric layer on a semiconductor substrate;

forming and patterning a conductive layer on the dielectric layer to define the RF component;

forming a plurality of openings on opposing sides and through the dielectric layer at least to the semiconductor substrate the openings having a diameter ranging from about 0.5 to about 20 microns and substantially uniform spacing between adjacent openings in a range of about 20 to about 200 microns; and

releasing the RF component from the semiconductor substrate by exposing the semiconductor substrate to a dry [an] etchant comprising XeF_2 passing through the openings to the semiconductor substrate.

(8) Kindly cancel Claims 15-16, 18-19 without prejudice or disclaimer.

(9) Kindly amend Claim 23 as follows:

23. (Amended) A method for making a radio frequency (RF) component comprising:

forming a dielectric layer on a semiconductor substrate;

forming and patterning a conductive layer on the dielectric layer to define the RF component;

forming a plurality of openings on opposing sides and through the dielectric layer in a predetermined pattern at least to the semiconductor substrate the openings having a diameter ranging from about 0.5 to about 20 microns and substantially uniform spacing between adjacent openings in a range of about 20 to about 200 microns; and

releasing the RF component from the semiconductor substrate by exposing the semiconductor passing through substrate to a dry [an] etchant comprising XeF2 passing the openings to the semiconductor substrate.

(10) Kindly cancel Claim 25 without prejudice or disclaimer.